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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Mun-Mo Jeong

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EXAMINER

GEBREMARIAM, SAMUEL A

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

1. Applicant's arguments, filed on 10/27/05, with respect to the final rejection have been fully considered and are persuasive. The finality of the last office action has been withdrawn. A new office action on the claims follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Bothra, US patent No., 6,281,585.

Regarding claim 26, APA teaches (fig. 1) a method for manufacturing a semiconductor device comprising: forming plural interconnection lines (fig. 1), each including an interconnection layer (14) and a capping layer (16) on a semiconductor substrate (10); forming an interlayer insulating layer (18) overlying the plural interconnection lines, wherein the thickness of a portion of the interlayer insulating layer on one of the capping layers is different from the thickness of a portion of the interlayer insulating layer on the others (refer to fig. 1); first etching the interlayer insulating layer to form first contact holes (20a, 20b and 20c) therein using a first etchant having a high etching selectivity between the capping layer and the interlayer insulating layer; and forming a conductive layer (contact holes are formed for forming conductive layer) within the contact holes, wherein the interconnection layer (14) and the capping layer

(16), are formed by sequentially depositing a first material layer for interconnection (14), and a second material layer for capping (16), and patterning the second material layer.

APA does not explicitly teach forming an etching stopper, using a first etchant having a high etching selectivity between the etching stopper and the interlayer insulating layer; second etching a portion of each etching stopper exposed by the first contact holes, using a second etchant having a low etching selectivity between the etching stopper and the capping layer, thereby forming second contact holes; and the etching stopper is formed by depositing a third material layer, and then patterning the third material layer and then patterning the second and first material layers, using the patterned third material layer.

Bothra teaches (figs. 5A-5k) forming an interconnection layer (140b), a capping layer (140a), and an etching stopper (150, refer to fig. 5A) that are formed by sequentially depositing a first material layer for interconnection (140b) a second material layer for capping (140a), and a third material layer for stopping etching (150), patterning the third material layer (150, refer to fig. 5J) and then patterning the second (140a) and first material layers (140b), using the patterned third material layer (150, refer to 5K and col., lines 13-35). Bothra further teaches performing the etching process using two etching chemistry involving two different gases (col. 7, lines 25-35)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the etch stop layer taught by Bothra in the process of APA in order to form contact holes. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of

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forming the interconnection layer, the capping layer, and the etching stopper by sequentially depositing a first material for interconnection, a second material layer for capping and a third material layer for stopping etching, patterning the third material layer and then patterning the second and first material layers, using the patterned third layer as taught by Bothra in the process of APA in order to form via structures that are self aligned. Furthermore the combined process of APA and Bothra teaches performing a dry etching method using an etchant having a low etching selectivity between the etching stopper and the capping layer.

Regarding claim 27, APA teaches substantially the entire claimed method of claim 26 above including stopping etching when a top surface of each etching stopper is exposed.

The claimed limitation above is an inherent property of an etch stop layer. Therefore APA's process is capable of stopping etching when a top surface of each etching stopper is exposed.

Allowance

4. Claims 1-9, 11-13, 21 and 22 are allowed.

Reason for Allowance

5. The following is an examiner's statement of reasons for allowance: The prior art of record does not teach or suggest, singularly or in combination at least the limitation of "stopping etching when a top surface of each etching stopper is exposed... thereby forming second contact holes, and leaving the capping layers of the plural interconnection lines at a substantially the same thickness such that the contact

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resistances of the plural interconnection lines are substantially uniform" as recited in claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant's arguments with respect to claims 26-27 have been considered but they are moot in view of new grounds of rejection.

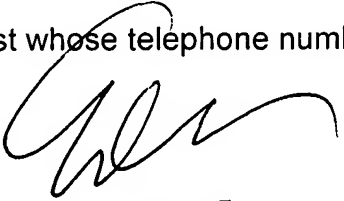
Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
March 6, 2006



EDDIE LEE
SUPERVISORY PATENT EXAMINER
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